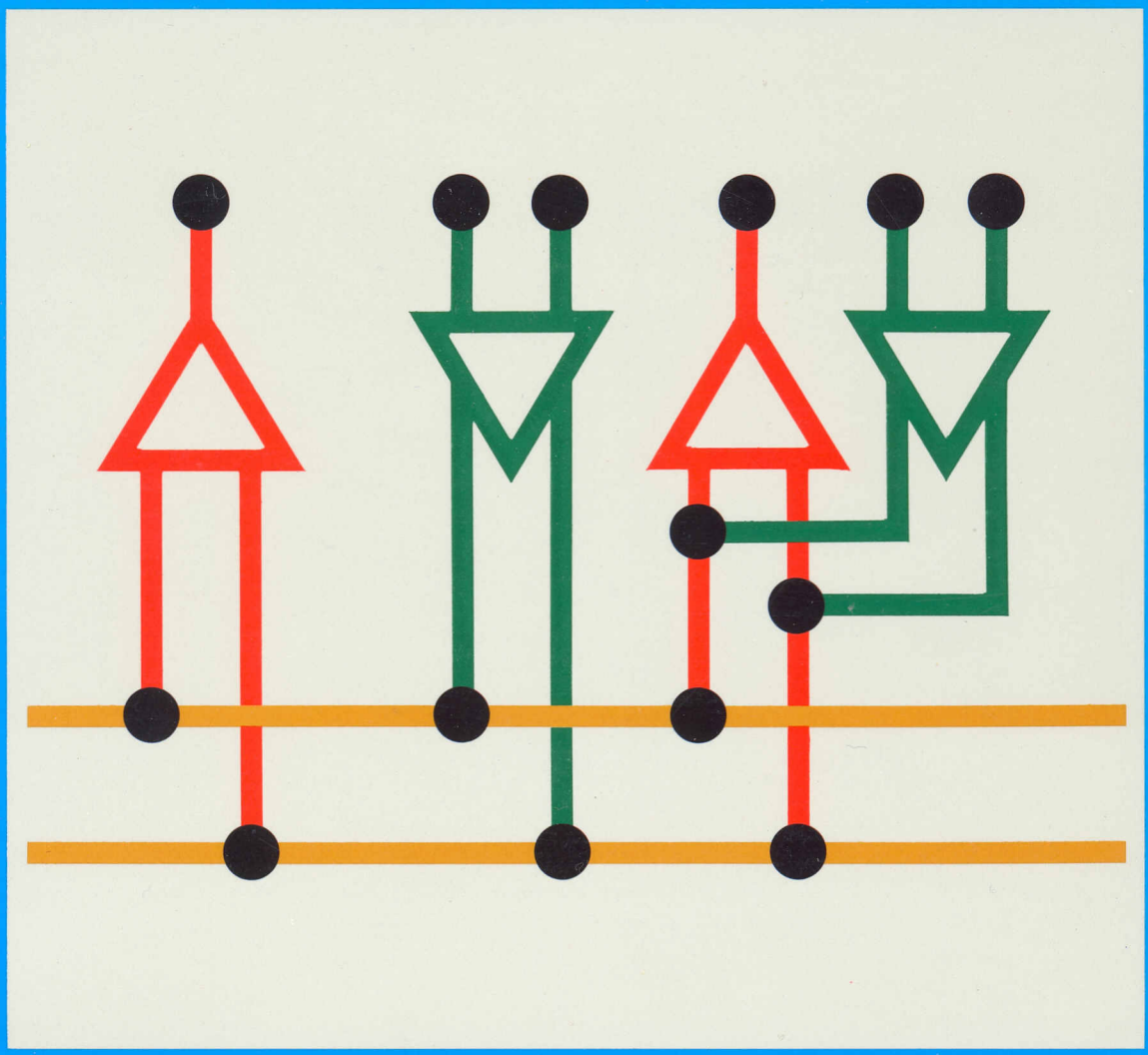
BRE428/D

STANDARD DIGITAL BUS INTERFACES



MOTOROLA

STANDARD DIGITAL BUS INTERFACES

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STANDARD DIGITAL BUS INTERFACES

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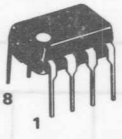
Increasingly, as ICs progress to larger levels of sophistication and more of a complex nature, cohesive elements are required to join common blocks into systems. Moreover, the need to interconnect individual pieces of equipment into complex systems has led to the establishment of several Interface Standards to ensure equipment compatibility.

This brochure serves to explain the salient characteristics of a number of both official and unofficial bus interface standards and to highlight the ICs in Motorola's offering designed to meet the requirements of a given specification.

Each section illustrates the common bus structures: single-wire or differential configuration, party line operation, bidirectionality, power supply requirements, and terminations. Also, second-source availability will be noted on the recommended IC elements.

PACKAGES



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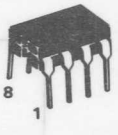
CASE 626



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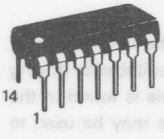

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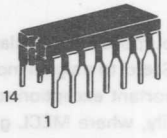

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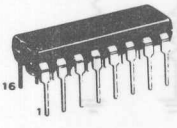

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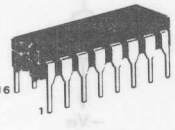

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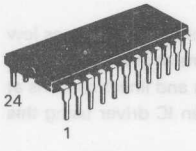

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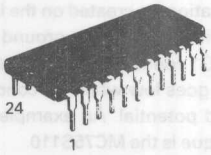

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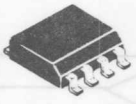

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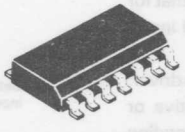
SO8 CASE 751 D SUFFIX



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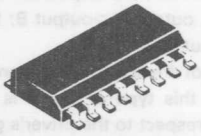

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SO16 CASE 751B D SUFFIX

TRANSMISSION SYSTEMS - A BRIEF REMINDER

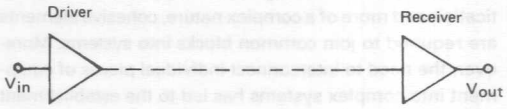
1.SYSTEM DESCRIPTION

A basic driver/receiver transmission system is shown in figure 1. An input data (V_{in}) feeds a driver which drives a line. At the other end of this line the receiver detects the information and provides an output data (V_{out}), usually of the same logic level as V_{in}.

The line involved can be a single line, a coaxial cable, a twisted pair line or a multi-cable. It can operate in a single ended or differential mode.

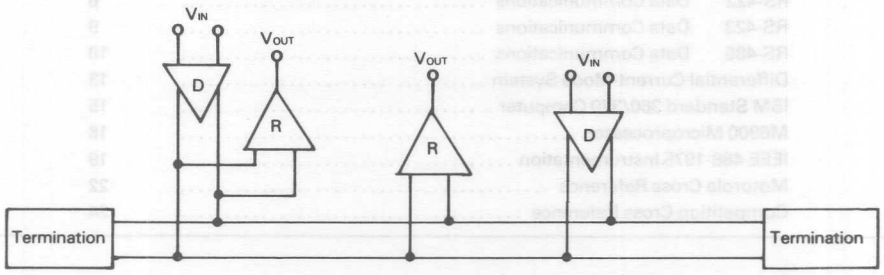
Another common driver/receiver system, shown in figure 2, is commonly called a party line or bus system.

FIGURE 1 - TYPICAL DRIVER RECEIVER SYSTEM



In this system, the line is shared by drivers, receivers and transceivers. It should be noticed that although any driver can be utilized to drive the line, only one driver can be used at any one time.

FIGURE 2 – TYPICAL "PARTY LINE" OR "BUS" SYSTEM



2. LINE DRIVER

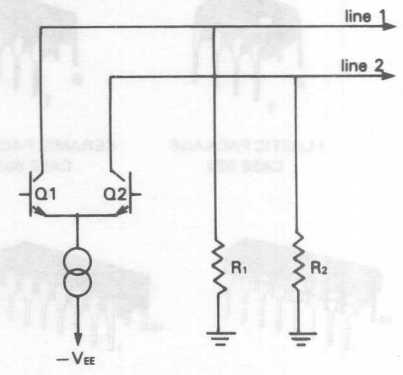
The line driver purpose is to translate the input logic level (DTL, TTL, CMOS, etc) to a signal more suitable for driving the line. An important exception to this is found in the MECL logic family, where MECL gates may be used to drive the line directly.

A popular method of driving lines between TTL systems is the differential open collector approach (see figure 3).

A differential voltage which is a function of the line terminations is created on the line.

One line is always at ground potential. Line 1 goes low when Q1 conducts and line 2 remains at ground potential. Line 2 goes low when Q2 conducts and line 1 remains at ground potential. An example of an IC driver using this technique is the MC75S110.

FIGURE 3 - DIFFERENTIAL OPEN COLLECTOR

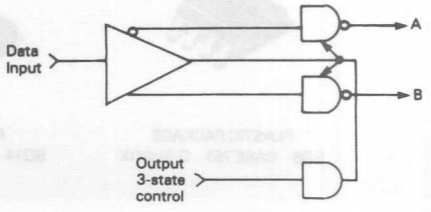


Other types of drivers include balanced differential voltage drivers (figure 4) such as the MC3487.

In this type of circuit, the outputs are switched so that for a logic 1 input, output A >output B; for a logic 0 input, output B >output A.

The third type of driver is the single-ended voltage driver. The output of this type of driver is either positive or negative, with respect to the driver's ground, depending on the input. Figure 5 shows this type of driver. Example of this type of driving: MC1488 or MC3488A.

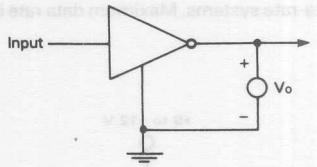
FIGURE 4 - MC3487 EQUIVALENT CIRCUIT BALANCED DIFFERENTIAL VOLTAGE DRIVER



3.LINE RECEIVER

The line receiver provides the reverse function of a line driver where the voltage previously applied to a line is now detected and restored to an output logic level. This function may be performed by various digital and linear ICs. Simple examples of this include comparators and gates. The latter includes a group of ICs specially designed as line receivers that combine linear and digital techniques. These ICs use linear circuitry to detect the output signal from the cable. This signal level may be quite small (less than 100 mV) with considerable noise. The digital circuits provide the necessary drive to interface with any of the common digital locic families, such as TTL, CMOS, MECL, etc.

FIGURE 5 - SINGLE-ENDED LINE DRIVER



Single ended line driver

4.NOISE CONSIDERATIONS

Noise is an important consideration in the line transmission of digital data. Where noise appears and how it influences the system will depend largely on the overall transmission line system used. Noise generally appears in two primary places in line driver/receiver systems : one, in the ground system, or two, directly on the line.
A simple single-ended system as shown in Fig. 1 is particularly prone to both ground and induced noise (from nearby equipment). One solution to this degradation is to increase the signal level, using high-threshold logic, which requires higher supply voltages.
In a differential system as shown in Fig. 2, externally-induced noise will appear equally on both inputs to the line receiver. The receiver uses a differential input stage to respond primarily to a differential signal, rejecting common-mode noise and providing a significant advantage over the single-ended approach.

5. PRODUCT SELECTION.

The actual selection of the line driver and receiver will depend on many factors including cost, power supply voltages, logic level, clock rate, length of line, etc.

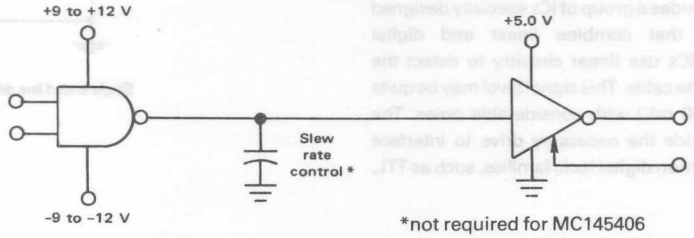
Available Motorola line drivers and receivers are shown in detail on the following pages and a competition cross refererice is availabe at the end of the brochure.

RS-232C DATA COMMUNICATIONS

EIA Standard RS-232C is an established specification defining the logic levels and impedances at the modern/terminal interface. This has been a well-accepted standard for low data-rate systems. Maximum data rate is about 20 kilobaud.

Employing a voltage-mode type driver, RS-232C requires dual polarity logic signals and power supplies. The data is unidirectional and not conducive to party-line operation. Hysteresis is generally employed in RS-232C receivers and a single power supply is required at the receiver end. Termination is not required.

FIGURE 6



*not required for MC145406

EIA RS-232C	
Driver Output Voltage (Z_L = 3 kΩ to 7 kΩ)	$15\ V \leq V_{OH} \leq 5.0\ V$ $-5.0\ V \geq V_{OL} \geq -15\ V$
Driver Output Voltage ($Z_L = \infty$)	$\lvert V_O \rvert < 25\ V$
Driver Output Impedance (Power Supplies = 0)	$Z_O > 300\ \Omega$
Driver Short-Circuit Current	$\lvert I_O \rvert < 0.5$ amp
Driver Slew Rate	$\frac{dv}{dt} < 30\ V/\mu s$
Receiver Input Impedance	$7\ k\Omega > R_{in} > 3\ k\Omega$
Receiver Input Voltage	$\lvert V_I \rvert < 25\ V$
Receiver Output with Open Input	Mark (high)
Receiver Output with 300 Ω to Gnd of Input	Mark (high)
Receiver Output with +3.0 V on Input	Space (low)
Receiver Output with -3.0 V on Input	Mark (high)
Baud Rate	BR ≤ 20 kilobaud

SUGGESTED ICs FOR IMPLENTATION

MC1488 - QUAD RS-232C DRIVER, OUTPUT CURRENT LIMITING

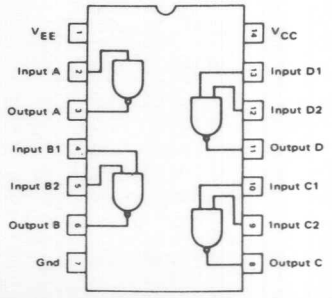
The MC1488 is a quad inverting TTL or DTL input line driver for RS-232C. It is designed to operate on ±9 to ±12 V power supplies and at a temperature range of 0 to 70°C.

Features include guaranteed power-off output impedance and output current limiting.

Packages: L Suffix - Case 632
P Suffix - Case 646
D Suffix - Case 751A

Second sources available

V_{OH} @ V_{CC}/V_{EE} = ±9.0 V Volts Min	V_{OL} @ V_{CC}/V_{EE} = ±9.0 V Volts Max	I_{OS} mA	t_{PHL} @ C_L = 15 pF ns Max
6.0	-6.0	±6.0 to 12	175

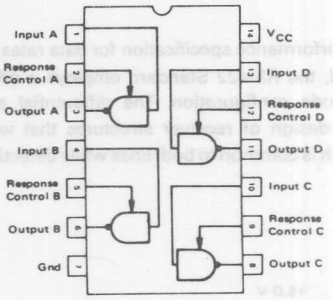


MC1489 - QUAD RS—232C RECEIVER, 0.25 V INPUT HYSTERESIS

The MC1489 quad inverting RS-232C receiver features 250 mV of input hysteresis. The threshold window may be shifted by means of the response control input.

Temperature range is 0 to 70°C and power supply requirement is a single +5 supply.

Packages: L Suffix - Case 632
P Suffix - Case 646
D Suffix - Case 751A



MC1489A - QUAD RS-232C RECEIVER, 1.1 V INPUT HYSTERESIS

The MC1489A is an improved version of the MC1489. It features 1.1 volts of input hysteresis for improved performance when slow-slewing input signals are present in noisy environments.

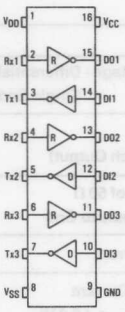
Second sources are available.

Device Number	Input V_{IHL} Volts	Input V_{ILH} Volts	t_{PHL} @ R_L = 390 Ω ns Max
MC1489	1.0 to 1.5	0.75 to 1.25	50
MC1489A	1.75 to 2.25	0.75 to 1.25	50

MC145406 - TRIPLE RS-232C DRIVER/RECEIVER

The MC145406 is a CMOS IC that combines 3 drivers and 3 receivers to provide an efficient low-power solution for RS-232C applications. It is designed to operate on +5 V to +12 V supplies and at a temperature range of -40° to +85°C. The drivers feature true TTL input compatibility, 300 Ohms power-off source impedance and output current limiting. The receivers can handle up to ±25 V, while presenting 3 to 7 KOhms impedance and have 800 mV of typical input hysteresis to improve noise immunity.

Packages : L Suffix - Case 620
P Suffix - Case 648



RECEIVERS

Input V_{IHL} Volts	Input V_{ILH} Volts	t_{PHL} @ C_L = 50pF ns max
1.35 to 2.35	0.75 to 1.25	300

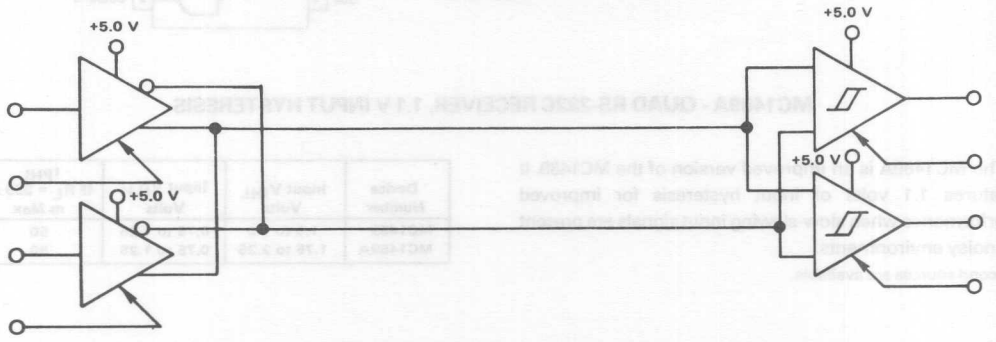
DRIVERS

V_{OH} @ V_{CC} = +5V Volts min	V_{OL} @ V_{CC} = +5V Volts max	I_{OS} @ V_{DD} = +12V, V_{SS} = -12V mA	t_{PHL} @ C_L = 50 pF R_L = 3kΩ ns max
@ V_{DD} = +5V V_{SS} = -5V 3.5	@ V_{DD} = +5V V_{SS} = -5V -4.0	@ $T_{X\ 1-3}$ to Gnd ± 10 to ± 20	325
@ V_{DD} = +12V V_{SS} = -12V 9.2	@ V_{DD} = +12V -10.0	@ $T_{X\ 1-3}$ to ± 15V ±40 to ±60	

RS-422 DATA COMMUNICATIONS

A high performance specification for data rates up to 10 megabaud, the RS-422 Standard employs a differential voltage-mode configuration. The differential approach facilitates design of receiver structures that will reject noise which is common to both lines while detecting small differential signals. Ground path potential difference problems are also effectively suppressed. In addition, the complementary differential driver outputs permit double the effective logic swing when operating on a single +5 V supply.

FIGURE 7



Three-State Drivers allow party line operation (only one may be enabled at a time).

EIA RS-422	
Driver Open-Circuit Voltage - Differential Single Ended	$\|V_{OD}\| \leq 6.0$ V $\|V_O\| \leq 6.0$ V
Driver Output Voltage $R_L = 50\ \Omega$ to Gnd (Each Output)	$2.0\text{ V} \leq \|V_{OD}\| \geq 0.5\ V_{OD}$ (Open Circuit) $\|\|V_{OD}\| - \|\overline{V_{OD}}\|\| \leq 0.4$ V
Voltage From Junction of 50 Ω Resistors tied to Outputs to Gnd	$\|\|V_{OS}\| - \|\overline{V_{OS}}\|\| \leq 0.4$ V
Driver Short-Circuit Current	$\|I_{SC}\| \leq 150$ mA
Driver Output Leakage Current ($V_{CC} = 0$, -0.25 V < V_O < +6.0 V)	$\|I_O\| \leq 100\ \mu$A
Driver Rise/Fall Times (10% + 90%) (Period of Output Pulse ≥ 200 ns) (Period of Output Pulse ≤ 200 ns)	 t_{TLH} or $t_{THL} \leq 0.1$ Output Period t_{TLH} or $t_{THL} \leq 20$ ns
Receiver Input Current (V_{CC} = On or Off) $V_I = \pm 10$ V $V_I = \pm 3.0$ V	 $I_I \leq \pm 3.25$ mA $I_I \leq \pm 1.50$ mA
Receiver Input Thresholds (-7.0 V ≤ V_{CM} ≤ +7.0 V)	$V_{TH} \leq \pm 200$ mV
Receiver Input Balance ($V_I = \pm 400$ mV thru Balanced 500 Ω resistors, -7.0 V ≤ V_{CM} ≤ +7.0 V)	Receiver Maintains Correct Logic State Output
Baud Rate	BR ≤ 10 megabaud

SUGGESTED ICs FOR IMPLEMENTATION

MC3486 - QUAD RS-422/423 RECEIVER

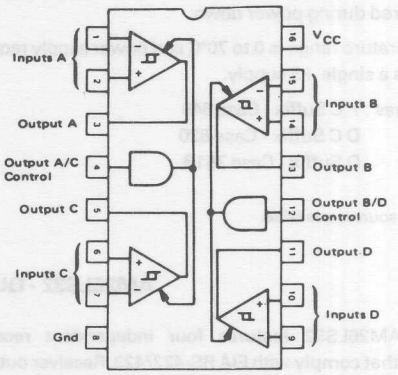
The MC3486 receiver outputs are 74 LS-compatible, three-state structures which are forced to a high-impedance state when the appropriate output control pin reaches a logic zero condtion. A PNP device buffers each output control pin to assure minimum loading for either logic one or logic zero inputs. In addition, each receiver chain has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms.

Temperature range is 0 to 70°C and power supply requirement is a single +5 supply.

Pakages : L Suffix - Case 620
P Suffix - Case 648
D Suffix - Case 751B

Second sources are available.

$V_{TH(D)}$ @ V_{ICM} = ±7.0 V Volts Max	I_{ID} @ V_{ID} = ±10 V V_{CC} = 0 to 5.25 V mA Max	t_{PHL}/t_{PLH} ns Typ	$t_{P(Control)}$ ns Typ
± 2.0	±3.25	20/25	25



MC3487 - QUAD RS-422 DRIVER

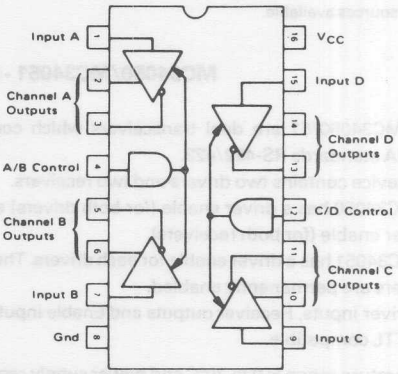
The MC3487 outputs are three-state structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. All input pins are PNP buffered to minimize input loading for either logic one or logic zero inputs. In addition, internal circuitry assures a high-impedance output state during the transition between power up and power down. Output sink/source current up to ±48 mA achievable.

Temperature range is 0 to 70°C and power supply requirement is a single +5 V supply.

Packages : L Suffix - Case 620
P Suffix - Case 648
D Suffix - Case 751B

Second sources available.

V_{OH} @ I_{OH} = 50 mA Volts Min	V_{OL} @ I_{OL} = 48 mA Volts Max	$V_{OD(Differential)}$ @ R_L = 100 Ω Volts Min	t_{PLH}/t_{PHL} ns Typ
2.0	0.5	2.0	15



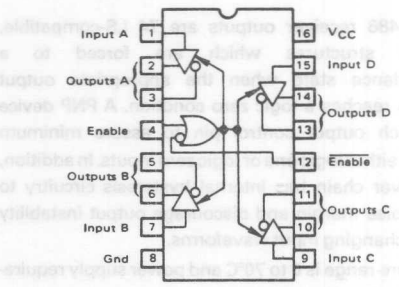
AM26LS31 - QUAD RS-422 DRIVER WITH THREE-STATE OUTPUTS

The AM26LS31 provides an enable/disable function common to all four drivers as opposed to the split enables on the MC3487 RS-422 driver. The high impedance output is assured during power down.

Temperature range is 0 to 70°C and power supply requirement is a single +5 supply.

Packages : P C Suffix - Case 648
D C Suffix - Case 620
D Suffix - Case 751B

Second sources available.



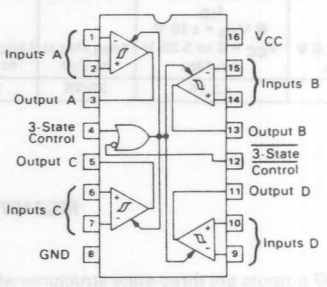
AM26LS32 - QUAD RS-422/423 RECEIVER

The AM26LS32 features four independent receiver chains that comply with EIA RS-422/423. Receiver outputs are 74LS compatible, three-state structures which are forced to a high impedance state when pin 4 is a logic "0" and pin 12 a logic "1". A PNP device buffers each output control pin to minimise loading for either logic "1" or logic "0" inputs. In addition, each receiver chain has an hysteresis input to improve noise margin and discourage output instability for slowly changing input waveforms.

Temperature range is 0 to 70°C and power supply requirement is a single +5 supply.

Packages : P C Suffix - Case 648
D C Suffix - Case 620
D Suffix - Case 751B

Second sources available.

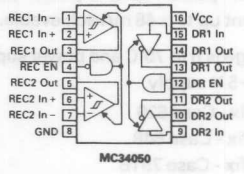


MC34050/MC34051 - DUAL RS-422/423 TRANSCEIVER

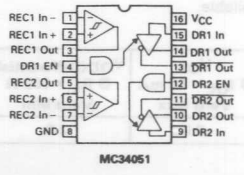
The MC34050/51 are dual transceivers which comply with EIA standards RS-422/423.
Each device contains two drivers and two receivers.
The MC34050 has a driver enable (for both drivers) and a receiver enable (for both receivers).
The MC34051 has a driver enable for each drivers. The two receivers are permanently enabled.
The Driver inputs, Receiver outputs and Enable inputs are 74LS TTL compatible.

Temperature range is 0 to 70°C and power supply requirement is a single +5 V supply.

Packages : L Suffix - Case 620
P Suffix - Case 648



MC34050



MC34051

RS-423 DATA COMMUNICATIONS

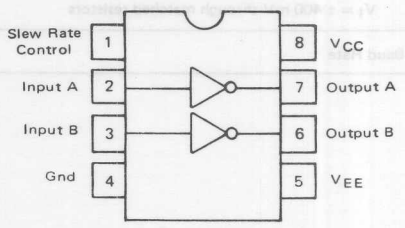
EIA Standard RS-423 is an improved version of RS-232C designed to meet or exceed all 232C requirements. As such it is single-wire, unidirectional, voltage-mode system with symmetrical power supply requirements (±).

EIA RS-423	
Driver Open-Circuit Voltage	$4.0\ V \leq V_{OH} \leq 6.0\ V$ $-4.0\ V \geq V_{OL} \geq -6.0\ V$
Driver Output Voltage (R_L = 450 Ω)	$\lvert V_O \rvert \geq 0.9\ V_O$ open circuit
Driver Short-Circuit Current	$\lvert I_{SC} \rvert \leq 150$ mA
Driver Output Current (Power Supplies = 0, $-6.0\ V \leq V_O \leq 6.0\ V$)	$\lvert I_O \rvert \leq 100\ \mu A$
Driver Rise & Fall Times ($t_{period} \geq 1.0$ ms) ($t_{period} \leq 1.0$ ms)	t_{TLH} or $t_{THL} \leq 300\ \mu s$ t_{TLH} or $t_{THL} \leq 0.3\ t_{period}$
Receiver Input Current (V_{CC} = 0 or +5.0 V) V_I = ± 10 V V_I = ± 3.0 V	 $I_I \leq \pm 3.25$ mA $I_I \leq \pm 1.5$ mA
Receiver Input Thresholds ($-7.0\ V \leq V_{CM} \leq 7.0\ V$)	$V_{TH} \leq \pm 200$ mV
Receiver Input Balance	Same as RS-422
Baud Rate	BR ≤ 100 kilobaud

SUGGESTED ICs FOR IMPLEMENTATION

MC34050/MC34051 - DUAL RS-422/423 TRANSCEIVER
MC3486 - QUAD RS422/423 RECEIVER
AM26LS32 - QUAD RS-422/423 RECEIVER
MC3488A - DUAL RS-423 DRIVER

The MC3488A is a dual voltage-mode driver with controlled slew rate. It is designed to operate on split power supplies in the range of ±9 to ±15 V.
Output current and slew rate is adjustable with the selection of an external resistor. Like the MC1488 driver, the MC3488A driver is inverting and the two output states are of opposite polarity.



Functionally equivalent to 9636.

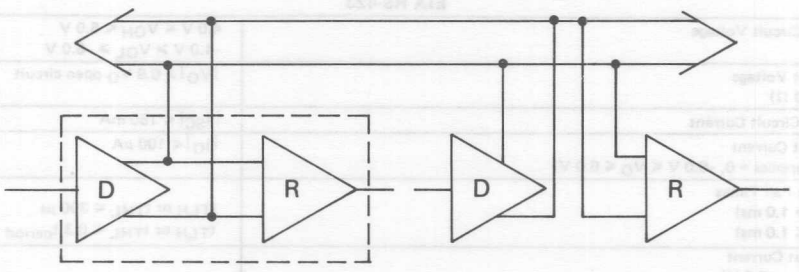
T_A = 0 to 70°C
Packages : P 1 Suffix - Case 626

RS-485 DATA COMMUNICATIONS

RS-485 was formulated by the EIA to meet increasingly complex applications for data communication systems. RS485 is an enhanced version of the differential line standard RS-422. RS-485 incorporates the specification of RS-422 as well as specifications on the use of multiple drivers and receivers.

As Fig. 8 illustrates, a multi point RS485 includes multiple drivers, receivers and transceivers.

FIGURE 8



As many as 32 driver/receiver pairs can be interconnected on an RS-485 party-line bus. When drivers contend with one another for access to the bus, dedicated circuitry within the IC's protects them from damage.

EIA RS-485	
Driver Open-Circuit Voltage Differential Single-ended	$1.5\ V < \lvert V_{OD} \rvert < 6\ V$ $0\ V < \lvert V_O \rvert < 6\ V$
Driver Output Voltage $R_L = 54\Omega$	$1.5\ V < V_t < 5.0\ V$
Voltage from Junction of 60Ω Resistors tied to output to ground	$\lVert V_t \rvert - \lvert \overline{V_t} \rVert < 0.2\ V$
Driver Rise/Fall Time (10 %o to 90 %o)	t_{TLH} or t_{THL} < 0.3 Output Period
Receiver Input Voltage Range	$-7\ V < V_I < 12\ V$
Receiver Input Balance $V_I = \pm 400$ mV through matched resistors	Receiver maintains correct logic state output
Baud Rate	BR ≤ 10 Megabaud

SUGGESTED ICs FOR IMPLEMENTATION

SN75172, SN75174 QUAD RS-485 LINE DRIVERS

The SN75172 and SN75174 are quad differential line drivers with three-state outputs.

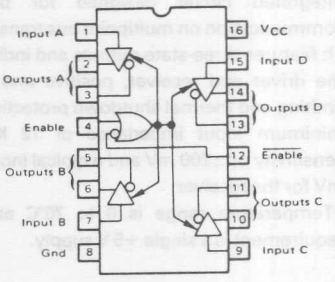
Each driver features wide positive and negative common-mode output voltage range making it suitable for party-line applications in noisy environments.

The SN75172/74 provide positive and negative current limiting and thermal shutdown for protection from line fault conditions on the transmission-bus line. Shutdown occurs at a junction temperate of approx. 150°C.

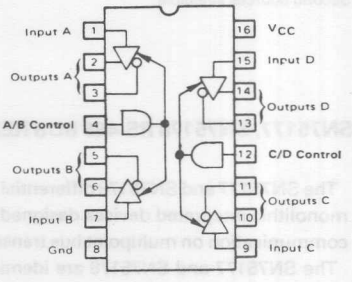
TA = 0 to 70°C
Packages : N Suffix - Case 648
J Suffix - Case 620

Second scources available

PIN CONNECTIONS SN75172



PIN CONNECTIONS SN75174



SN75173, SN75175 QUAD RS-485 LINE RECEIVERS

The SN75173 and SN75175 are quad differential line receivers with three-state outputs.

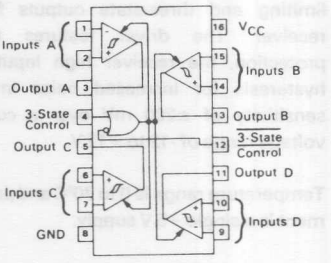
They allow balanced multipoint bus transmission at rates up to 10 Mbit/s. They feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over common-mode input voltage range of -12V to 12 V.

The SN75173/75 are designed for optimum performance when used with the SN75172 or SN75174 quadruple differential line receivers.

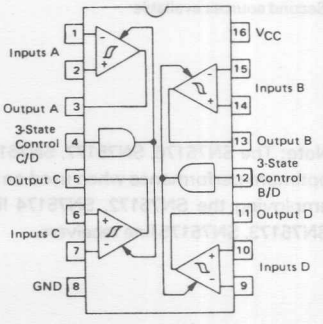
TA = 0 to 70°C
Packages : N Suffix - Case 648
J Suffix - Case 620

Second sources available

PIN CONNECTIONS SN75173



PIN CONNECTIONS SN75175



Note: SN75172, SN75174 and their respective receivers SN75173, SN75175 are direct plug-in replacements for RS 422 drivers and receivers including the AM26LS31, AM26LS32, MC3486 and MC3487. Thus you can convert an RS 422 system into an RS 485 party line by replacing the driver and receiver components.

SN75176 RS-485 BUS TRANSCEIVER *

The SN75176 differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus transmission lines.

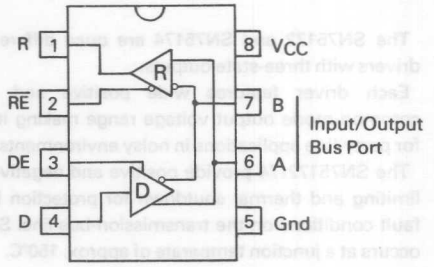
It features three-state outputs and individual enables for the driver and receiver, positive and negative current limiting and thermal shutdown protection for the driver, a minimum input impedance of 12 KOhms, an input sensitivity of ±200 mV and a typical input hysteresis of 50 mV for the receiver.

Temperature range is 0 to 70°C and power supply requirement is a single +5 V supply.

Packages : N Suffix - Case 626
J Suffix - Case 693

Second sources available

PIN CONNECTIONS



SN75176

SN75177, SN75178 RS-485 BUS REPEATERS *

The SN75177 and SN75178 differential bus repeaters are monolithic integrated devices designed for one-way data communication on multipoint bus transmission lines.

The SN75177 and SN75178 are identical except for the enable inputs, active-high for the SN75177, active-low for the SN75178.

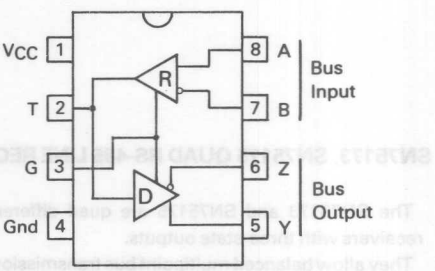
Both devices feature positive and negative current limiting and three-state outputs for the driver and receiver. The driver features thermal shutdown protection, the receiver high input impedance, input hysteresis for increased noise immunity and input sensitivity of ±200 mV over a common-mode input voltage range of -12 to +12 V.

Temperature range is 0 to 70°C and power supply requirement is a single +5 V supply.

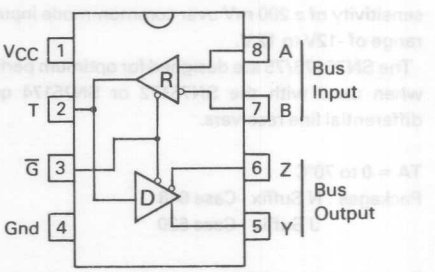
Packages : N Suffix - Case 626
J Suffix - Case 693

Second sources available

PIN CONNECTIONS



SN75177



SN75178

Note: The SN75176, SN75177, SN75178 are designed for optimum performance when used on transmission buses employing the SN75172, SN75174 line drivers and the SN75173, SN75175 line receivers.

*Device to be introduced at time of printing.

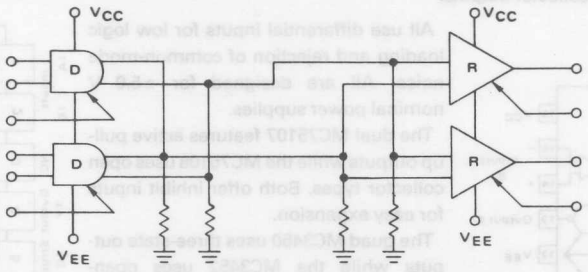
DIFFERENTIAL CURRENT-MODE SYSTEM

An unofficial standard for data transmission over generous lengths of either twisted-pair or coaxial cable. Lengths up to a mile are practical.

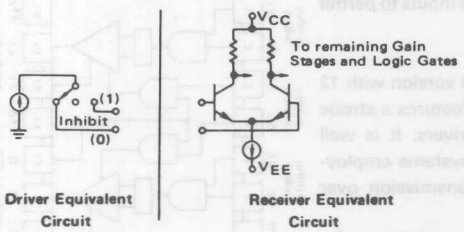
A current source (or sink) is switched between the pair of lines in response to the applied input logic condition. The current sources are designed to operate over a wide range of voltage compliance. Party line systems employing several drivers are configured by shutting off all but one of the current sources with appropriate Enable inputs.

Differential receivers are employed to detect the voltage generated by the driver current flowing through the required termination resistors. Differential receivers can sense correctly a few millivolts even when superimposed on up to ±3.5 V of common mode noise.

A unidirectional, current-mode system generally employing split power supplies for both driver and receiver. Party-lines systems may be configured easily.



CURRENT MODE	
DRIVERS	
Configuration	Switched Current Source, Differential Lines
Output Current	6 or 12 mA nominal
Output Compliance Range	-3.0 V to +10 V
Output Leakage Current	100 μA max
RECEIVERS	
Configuration	Differential Amplifier Input; Open Collector or Active Pull-up Outputs
Input Thresholds	±25 mV max
Common Mode Range	±3.0 V max
Differential Voltage Range	±5.0 V max
Input Current (V_{ID} = 0.5 V, V_{IC} = ±3.0 V) (V_{ID} = -2.0 V, V_{IC} = ±3.0 V)	 75 μA max -10 μA



For longer cable lengths or noisier environments, the added noise immunity available with differential mode systems is highly desirable. This system is satisfactory for line lengths beyond a mile. In a current-mode system, an active current source is switched between one or the other of two lines. A differential input receiver that rejects noise appearing common mode to both inputs is often used. Thus, the receiver can guarantee a given logic output with only ±20 mV of differential signal despite up to ±3.5 V of common mode noise. By inhibiting the current source on unused drivers, party line systems with multiple drivers and receivers can be constructed sharing a single pair of lines, thus saving considerable hardware in many systems.

SUGGESTED ICs FOR IMPLEMENTATION

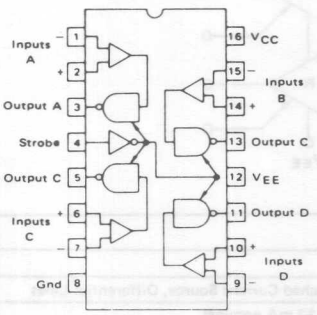
Quad Devices:
T_A = 0 to 70°C
Package: P Suffix - Case 648

Dual Devices:
T_A = o to 70°C
Package: P Suffix - Case 646

RECEIVERS

MC3450 - Quad; active pull-up outputs; common three-state enable.
MC3452 - Quad; open collector outputs.

MC75107 - Dual; active pull-up output.
MC75108 - Dual; open collector output.

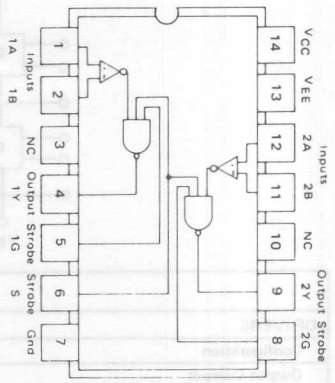


All use differential inputs for low logic loading and rejection of common-mode noise. All are designed for ±5.0 V nominal power supplies.

The dual MC75107 features active pull-up outputs while the MC75108 uses open collector types. Both offer inhibit inputs for easy expansion.

The quad MC3450 uses three-state outputs while the MC3452 uses open-collector outputs. Both have a single enable input for expansion/three-state bus capability.

Second source available for 75107-108. Second source for MC3450-52 is DS3650-52.



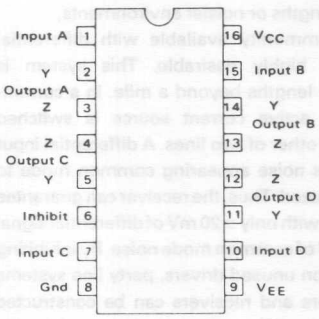
ALL RECEIVERS

Input V_{TH} mV Max	I_{IH} @ V_{ID} = 0.5 V µA Max	I_{IL} @ V_{ID} = -2.0 V µA Max	t_{PLH} ns Max
±25	75	-10	25

DRIVERS

MC3453 - Quad; common inhibit input; current sink approximately 12 mA.

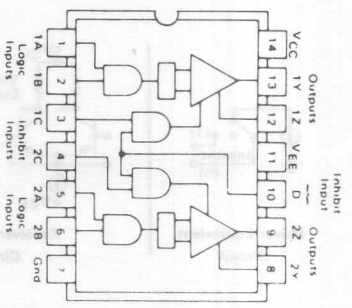
MC75S110 - Dual; industry standard.



The MC75S110 is a 12 mA dual current mode driver, with strobe inputs to permit party-line systems.

The MC3453 is a quad version with 12 mA current sources. It features a strobe common to all four drivers. It is well suited to high-density systems employing bit-parallel data transmission over long line lengths.

Second sources available for MC75S110 type.



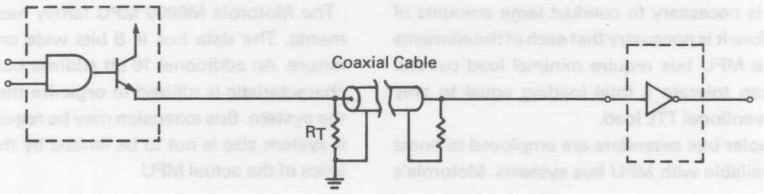
BOTH DRIVERS

$I_{O\ (on)}$ mA Min	$I_{O\ (off)}$ µA Max	t_{PHL} ns Max
6.5	100	15

IBM STANDARD 360/370 COMPUTER

This specification covers the I/O on IBM 360/370 series computer systems. This standard may be used to interface add-on memories or disk storage controllers to IBM systems. The interface is bit parallel and bidirectional. A number of stringent fault condition and power-off requirements are included in the specification

TYPICAL APPLICATION



IBM GA-22-6974-0	
Structure	Uncommitted Emitter Drivers Hysteresis-Equipped Receivers
Driver Output Voltage - High Logic State (I_{OH} = - 59.3 mA)	3.11 V min
Driver Output Current - Low Logic State (V_{OL} = - 0.15 V)	- 240 μA max
Driver Output Reverse Leakage Current - Low Logic State (V_O = 3.0 V, V_{CC} = OV)	40 μA max
Receiver Input Voltage High Logic State Low Logic State	 1.7 V min 0.7 mxa
Receiver Input Hysteresis	0.2 V min
Receiver Input Current (V_{IH} = 3.11 V) (V_{IH} = 7.0V) (V_{IH} = 6.0 V, V_{CC} = O V)	 0.17 mA 5.0 mA 5.0 mA

SUGGESTED ICs FOR IMPLEMENTATION

MC3481, MC3485 QUAD DRIVERS

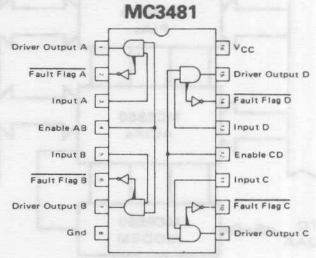
Both devices:
T_A = 0 to 70°C
Packages: P Suffix - Case 648

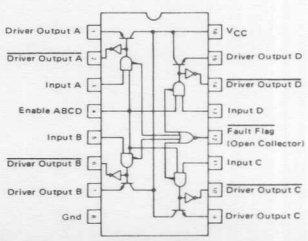
The MC3481 and MC3485 are quad single-ended line drivers specifically designed to meet the IBM 360/370 I/O specification (GA22-6974-3).

Output levels are guaranteed over the full range of output load and fault conditions. Compliance with the IBM requirements for fault protection, flagging and power up/power down protection for the bus make this an ideal line driver for party line operations.

The MC3481 has dual enable and individual fault flag.
The MC3485 has common enable and common fault flag; LS Totem pole Driver Output

MC3481





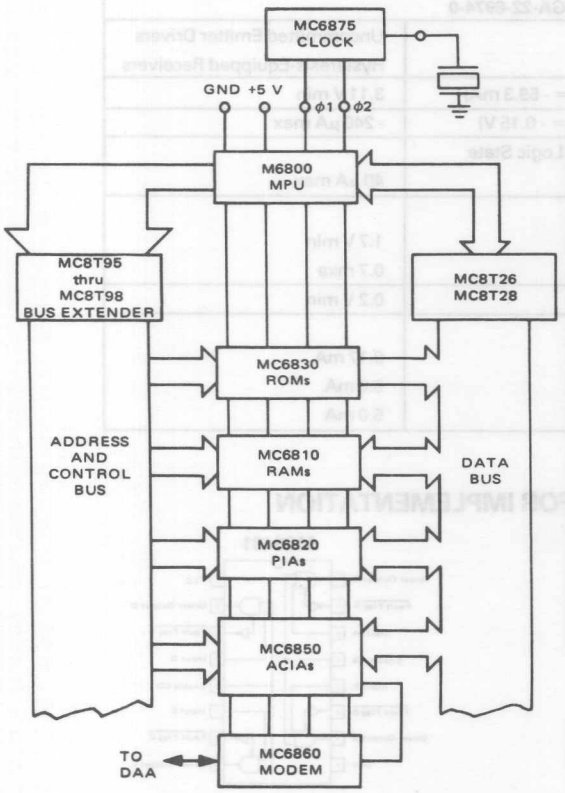
MC3485

M6800 MICROPROCESSOR

The revolutionary M6800 is a bus organized system. The requirements on the microprocessor bus are especially stringent since the M6800 is fabricated utilizing NMOS technology with its attendant high circuit density characteristics. However, MOS structures become unduly large when it is necessary to conduct large amounts of current. Therefore it is necessary that each of the elements attached to the MPU bus require minimal load current. This system can tolerate a total loading equal to only about one conventional TTL load.

Generally bipolar bus extenders are employed to boost the loading available with MPU bus systems. Motorola's MPU bus extenders employ Schottky technology with high-impedance PNP inputs which present a low current loading to the MPU while retaining good speed performance. An advanced noble metal Schottky barrier system is employed to assure good long-term stability.

The Motorola M6800 MPU family has two bus requirements. The data bus is 8 bits wide and bidirectional in nature. An additional 16 bit address bus of unidirectional characteristic is utilized to organize the memory used in the system. Bus extension may be required on both buses if system size is not to be limited by the drive characteristics of the actual MPU.



M6800	
Input Voltage	
High Logic State	V_{SS} +2.0 V to V_{CC}
Low Logic State	V_{SS} +0.3 V to V_{SS} to V_{SS} +0.8 V
Input Logic Current	2.5 μA max @ 0 to 5.25 V
Output Voltage - High Logic State	V_{SS} +2.4 V min
Data Bus (R_L = 11.7 kΩ, C_L = 130 pF)	
Address Bus (R_L = 16.5 kΩ, C_L = 90 pF)	
Output Voltage - Low Logic State	V_{SS} +0.4 V max
Data Bus (R_L = 11.7 kΩ, C_L = 130 pF)	
Address Bus (R_L = 16.5 kΩ, C_L = 90 pF)	
Capacitance	
Data Lines	12.5 pF max
Address Lines	12.0 pF max
Three-State Leakage Current	
Data Bus	10 μA max @ 0.4 to 2.4 V
Address Bus	100 μA max @ 5.25 V

SUGGESTED ICs FOR IMPLEMENTATION

All devices (except the MC26S10):
T_A = 0 to 75°C

Packages : L Suffix - Case 620
P Suffix - Case 648

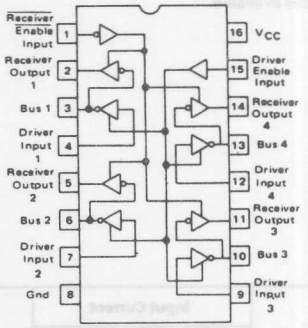
For the MC26S10, T_A = 0 to 70°C and Package is P Suffix - Case 648 only

DATA BUS
MC8T26A - QUAD INVERTING BUS EXTENDER
MC8T28 - NON-INVERTING BUS EXTENDER

A quad bidirectional extender employing PNP-buffered inputs for low logic loading and MOS compatibility. Three-state output structures are used for bus compatibility. Driver outputs can sink 48 mA while receiver outputs sink 20 mA at 0.5 V. Driver Enable and Receiver Enable can be tied together to achieve Read/Write function.

8T28 is identical to 8T26A, but with non-inverting logic.

Second sources available.

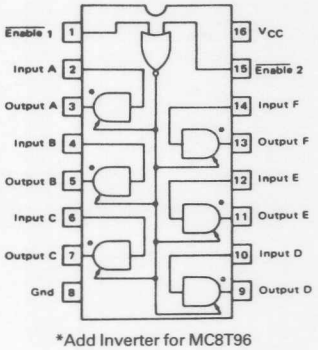


ADDRESS BUS
MC8T95 - HEX BUFFER
MC8T96 - HEX INVERTING BUFFER
MC8T97 - HEX BUFFER
MC8T98 - HEX INVERTING BUFFER

Six unidirectional bus extenders in a single package with PNP-buffered inputs and three-state outputs. The devices differ in their enable logic and inverting logic.

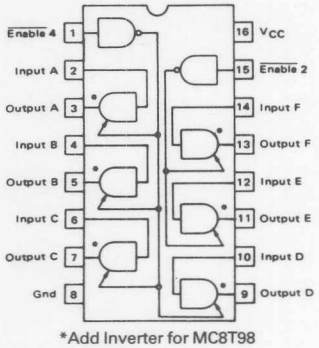
Second sources available.

MC8T95



*Add Inverter for MC8T96

MC8T97



*Add Inverter for MC8T98

V_{OL} @ I_{OL} = 48 mA Volts Max	V_{OH} @ I_{OH} = -5.2 mA Volts Min	I_{OS} mA Typ	t_{PLH} ns Typ	$t_{P(Enable)}$ ns Typ
0.5	2.4	-80	6.0	11

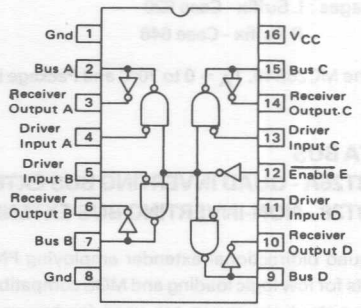
SUGGESTED ICs FOR IMPLEMENTATION (continued)

MC26S10 QUAD OPEN-COLLECTOR BUS TRANSCEIVER

This quad transceiver is designed to interface SHOTTKY TTL or NMOS logic to a low impedance bus. The driver (Bus) output is open collector and can sink up to 100 mA at 0.8 V. An active low Enable controls all four drivers allowing the outputs of different device drivers to be connected together for party line operation.

Second sources available.

PIN CONNECTIONS



Device Number	Input Current		I_{OHL} Output Disabled Leakage Current - High Logic State μA Max	t_{PLH}, t_{PHL} Propagation Delay Time - High to Low or Low to High ns Max
	I_{IH} μA Max	I_{IL} μA Max		
MC8T26A	25	-200	100	14
MC8T28	25	-200	100	17
MC26S10	30	-540	100	15

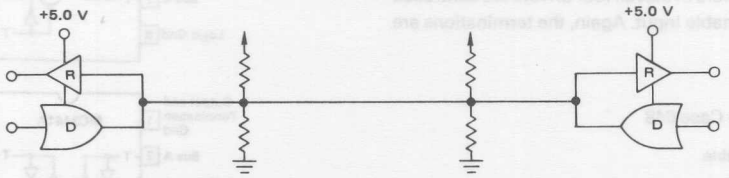
IEEE 488-1978 INSTRUMENTATION

There is an increasing trend in the instrumentation industry to consider implementation of the total system instead of individual instruments. The rapid trend to automated testing systems controlled by a minicomputer or programmable calculator has encouraged designed-in provisions for interconnecting individual instruments.

The problem has been complicated, however, by the diversity of internal logic architectures, the range of size and complexities required in these systems and the multitude of individual manufacturers involved.

Steps toward standardization of the instrumentation interface bus have been made by the IEEE with Standard 488-1978. Acceptance of this Standard now permits interconnection of many types of measurement apparatus, manufactured by numerous firms, into complex systems, simply by plugging in connecting cables.

The general purpose interface bus (G.P.I.B.) is a bit-parallel, byte-serial, computer-compatible bus. The sixteen lines associated with the system consist of eight data lines, permitting parallel transmission of ASCII characters, three "handshake" lines for control of data transfers and five general bus management control lines.



IEEE 488-1978	
Number of Devices	15 per system max
Number of Signal Lines	8 data, 8 control
Data Rate	1 Megabyte max
Transmission Path	20 meters total accumulated cable length max
Data Transfer	Byte-serial, bit-parallel, bidirectional, using interlocked handshake technique
Driver Configuration	Open collector for SRQ, NRFD, NDAC Open collector or three-state for DIO 1-8, DAV, IFC, ATN, REN and EOI
Driver Output Voltage Low Logic State (I_{OL} = 48 mA) High Logic State Three-State (I_{OH} = -5.2 mA) Open Collector (V_O = 5.25 V)	 $V_{OL} \leq 0.5$* 2.4 V min $I_{Leakage}$ = 0.25 mA
Third State Leakage Current (V_O = 2.4 V)	±40 μA max
Receiver Input Thresholds Low Logic State High Logic State	 ≤ 0.8 V ≥ 2.0V
Receiver Thresholds (If Schmitt Trigger used) Low Logic State High Logic State Hysteresis	 +1.1 V > V_{TH} - > 0.6 V +2.0 V > V_{TH} + > 1.5V ≥ 0.4 V
Resistive Termination Recommendations	3.0 kΩ to V_{CC} 6.2 kΩ to Gnd
Receiver Input Current Low Logic State (V_{IL} = 0.4 V) High Logic State (V_{IH} = 2.4 V) (V_{IH} = 5.25 V)	 -1.6 mA max +40 μA max +1.0 mA max
DC Load Characteristics (I ≤ 0 mA) (I ≥ 0 mA) (I ≥ -12 mA) (V ≤ 0.4 V) (V ≥ 0.4 V) (V ≤ 5.5 V) (V ≥ 5.0 V)	 V < 3.7 V V > 2.5 V V > -1.5 V (if receiver present) I < 1.3 mA I > -3.2 mA I < 2.5 mA I > 0.7 mA or small-signal Z must be ≤ @ 1 MHz

*The IEEE 488-1978 Bus Standard changes $V_{OL(D)}$ from 0.4 to 0.5 V maximum to permit the use of Schottky technology.

SUGGESTED ICs FOR IMPLEMENTATION

MC3440A, MC3441A, MC3446A, MC3448A QUAD TRANSCEIVERS

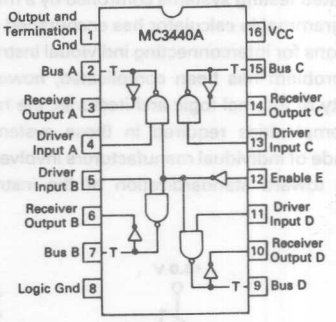
Quad bidirectional voltage-mode transceivers featuring open-collector drivers and hysteresis-equipped receivers and TTL compatible. The MC3440A and the MC3441A provide the required termination resistors on the bus terminal.

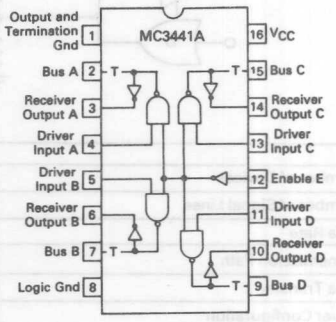
The MC3440A version consists of three drivers controlled by a common Enable input and a single driver without an Enable input. Terminations are provided in the device.

The MC3441A differs in that all four drivers are controlled by the common Enable input. Again, the terminations are provided.

T_A = 0 to 70°C
Package: P Suffix - Case 648

Second source available.



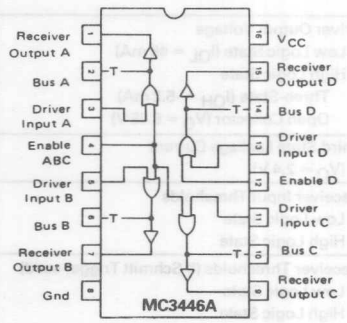


Intended for low-power applications or instruments using CMOS logic, the MC3446A provides the required termination resistors and two Enables: one for three drivers and another for the remaining driver.

Driver and Enable inputs feature low logic loading. Hysteresis is provided on the receiver for improved noise margin. Power up/down protection provided.

T_A = 0 to 70°C
Package: P Suffix - Case 648

Second sources available.

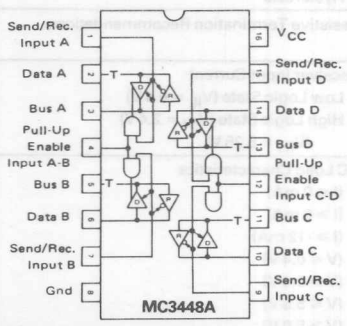


Designed for systems using bidirectional architecture such as those using microprocessors, the MC3448A contains four complete channels. Each channel features a three-state driver with a pull-up Enable which can be used to simulate the open-collector configuration, a Schmitt-trigger-equipped receiver with three-state output and the required bus termination.

PNP-buffering is provided on all logic inputs for MOS or MPU compatibility. Power up/down protection provided.

T_A = 0 to 70°C
Packages: P Suffix - Case 648
L Suffix - Case 620

Second sources available



Device Number	Receiver Input Hysteresis mV Min	Driver Output Voltage @ I_{OL} = 48 mA Volts Max	Bus Divider Voltage Volts	t_{PHL} (Driver or Receiver) ns Max
MC3440A	400	0.5	2.5 to 3.7	30
MC3441A	400	0.5	2.5 to 3.7	30
MC3446A	400	0.5	2.5 to 3.7	50
MC3448A	400	0.5	2.75 to 3.7	23

Note: See MC68488 for logic implementation of GPIB.

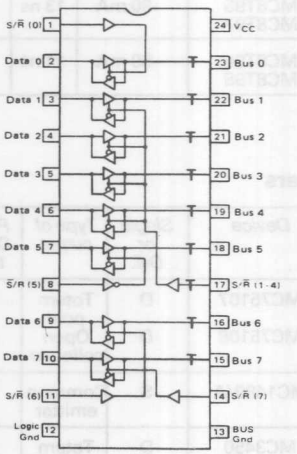
MC3447 - OCTAL TRANSCEIVER

T_A = 0 to 70°C
Packages : L Suffix - Case 623
P Suffix - Case 649

This bidirectional bus transceiver is intended as the interface between TTL or MOS logic and the IEEE Standard Instrumentation Bus (488-1978, often referred to as GPIB). The required bus termination is internally provided.

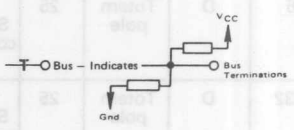
Low power consumption has been achieved by trading a minimum of speed for low current drain on non-critical channels. A fast channel is provided for critical ATN and EOI paths.

Each driver/receiver pair forms the complete interface between the bus and an instrument. Either the driver or the receiver of each channel is enabled by a Send/Receive input with the disabled output of the pair forced to a high impedance state. The receivers have input hysteresis to improve noise margin, and their input loading follows the bus standard specifications.



Device Number	Receiver Input Hysteresis mV Min	Drive Output Voltage @ I_{OL} = 48 mA Volts Max	t_{PHL} (Driver or Receiver) ns Max
MC3447	400	0.5	30 (D) 22 (R) *

*Fast Channel.



CROSS-REFERENCE

Drivers

	Device	Output current Capability	Prop. Delay Time	Single or Diff.	Party Line Operat.	Strobe or Enable	Power Supply	Logic Compati-bility	Corresponding receiver	Additional Features
DUAL	MC3488A	150mA	-	S	-	-	from ± 9V to + 15V	TTL/DTL	MC3486	RS423 and RS232C
	MC75S110	12 mA	15 ns	Diff.	Yes	S	± 5 V	TTL	MC75107 MC 75108	TTL input compatibility Schottky processing Inhibitor available for driver selection
QUAD	MC1488	10 mA	175 ns	S	-	-	± 15 V	TTL/DTL	MC1489,A	Power-off source impedance 300 Ω min RS232C Simple slew rate control with external capacitor
	MC3453	12 mA	15 ns	Diff.	Yes	S	± 5 V	TTL	MC3450 MC3452	Four independent drivers - 3 V output common mode voltage over active operating range
	MC3487	48 mA	15 ns	Diff.	-	E	+ 5 V	TTL/DTL	MC3486	Schottky process RS422 Three state outputs
	MC3481 MC3485	60 mA	25 ns	S	Yes	E	+ 5 V	TTL	-	Compliance with IBM 360 370 Schottky processing. Separate enable and fault flag 3481. Common enable and fault flag 3485
	AM26LS31	150 mA	20 ns	Diff.	-	E	+ 5 V	MOS/TTL	AM26LS32	RS422 Spec Schottky processing Mos compatible
	SN75172	60 mA	15 ns	Diff.	Yes	E	+ 5 V	MOS/TTL	SN75173	RS422 and RS485 Plug-in replacement for AM26LS31
	SN75174	60 mA	15 ns	Diff.	Yes	E	+ 5 V	MOS/TTL	SN75175	RS422 and RS485 Plug-in replacement for MC3487
HEX	MC8T95 MC8T97	-80 mA	13 ns	S	Yes	E	+ 5 V	MOS/TTL	-	High speed Schottky technology M6800 compatible. 8T96 and 8T98 inverting 8T95 and 8T97 non inverting
	MC8T96 MC8T98	-80 mA	11 ns	S	Yes	E	+ 5 V	MOS/TTL	-	

Receivers

	Device	Single or Diff.	Type of output	Prop. Delay time	Strobe or enable	Power Supply	Logic compatibility	Corresponding Driver	Additional Features
DUAL	MC75107	D	Totem pole	25	S	± 5 V	TTL/DTL	MC75S110	Input sensitivity ± 25 mV Differential input common-mode voltage range of ± 30 V TTL or DTL drive capability
	MC75108	D	Open collector	25	S	± 5 V	TTL/DTL	MC75S110	
QUAD	MC1489/A	S	Common emitter	50	-	+ 5 V	TTL/DTL	MC1488	Meets EIA Standard RS232C
	MC3450	D	Totem pole	25	S	± 5 V	TTL	MC3453	Receiver performance identical to the MC75107/108 Four independent receivers Implied "AND" capability with open collector outputs (MC3452)
	MC3452	D	Open collector	25	S	± 5 V	TTL	MC3453	
	MC3486	D	Totem pole	25	3 State control	+ 5 V	TTL/DTL	MC3487 MC3488A	Meets RS422/423 specification Receiver output 74LS compatible Four independent drains Internal hysteresis
	AM26LS32	D	Totem pole	25	3 State control	+ 5V	TTL	AM26LS31	Meets RS 422/423 Spec Three state drive, with choice of complementary output enables, for receiving directly onto a data bus
	SN75173	D	Totem pole	25	3 State control	+ 5V	TTL	SN75172	Meets RS 422/423 and RS 485 Spec. Plug-in replacement for AM26LS32
	SN75175	D	Totem pole	25	3 State control	+ 5V	TTL	SN75174	Meets RS 422/423 and RS 485 Spec. Plug-in replacement for MC 3486

Transceivers

	Device	Driver Characteristics			Receiver Char.		Additional Features
		Output Current	TPDT max	Strobe or Enable	TPDT max	Enable	
SINGLE	SN75176	60mA	15 ns	E	25 ns	Yes	Meets RS-485 Spec.
	SN75177/78	60mA	15 ns	E	25 ns	Yes	
DUAL	MC34050	-150 mA	20 ns	E	40 ns	Yes	Meets RS-422 Spec.
	MC34051	-150mA	20 ns	E	40 ns	-	
TRI	MC145406	60 mA	325 ns	-	300 ns	-	Meets RS-232C Spec. CMOS technology
QUAD	MC8T26A	-48mA	14 ns	E	14 ns	Yes	High speed schottky tech. Compatible 6800 microproc. 8T26A inv/8T28 non inv.
	MC8T28	-48 mA	17 ns	E	17 ns	Yes	
	MC26S10	100 mA	10 ns	E	10 ns	Yes	Schottky processing for high speed
	MC3440A	48 mA	30 ns	E	30 ns	Yes	Meets standards IEEE and IEC on instruments interface (488-1978). Electrical compatibility with General Purpose Interface Bus (GPIB). High input impedance.
	MC3441A	48 mA	30 ns	E	30 ns	Yes	
	MC3446A	48 mA	50 ns	E	50 ns	Yes	
	MC3448A	48 mA	15 ns	E	25 ns	Yes	
OCTAL	MC3447	48 mA	15 ns	E	30 ns channel 6 50 other channels	Yes	IEE standard 488-1978 TTL compatible receiver output. Three state output. High input impedance

COMPETITION CROSS REFERENCE	
Texas Instruments	*Motorola Direct Replacement*
AM26S10CN	MC26S10P
AM26LS31DC	AM26LS31DC
AM26LS31PC	AM26LS31PC
AM26LS32DC	AM26LS32DC
AM26LS32PC	AM26LS32PC
MC3446N	MC3446AP
MC3486J	MC3486L
MC3486N	MC3486P
MC3487J	MC3487L
MC3487N	MC3487P
μA9636ACP	MC3488AP1
N8T26AJ	MC8T26AL
N8T26AN	MC8T26AP
SN75107AJ	MC75107L
SN75107AN	MC75107P
SN75108AJ	MC75108L
SN75108AN	MC75108P
SN75126N	MC3481P
SN75130N	MC3485P
SN75172N/J	SN75172N/J
SN75173N/J	SN75173N/J
SN75174N/J	SN75174N/J
SN75175N/J	SN75175N/J
SN75176N/J	SN75176N/J
SN75177N/J	SN75177N/J
SN75178N/J	SN75178N/J
SN75188J	MC1488L
SN75188N	MC1488P
SN75189AJ	MC1489AL
SN75189AN	MC1489AP
SN75189J	MC1489L
SN75189N	MC1489P

COMPETITION CROSS REFERENCE	
National	*Motorola Direct Replacement*
DS1488 J	MC1488 L
DS1488 N	MC1488 P
DS1489 AJ	MC1489 AL
DS1489 AN	MC1489AP
DS1489 J	MC1489 L
DS1489 N	MC1489 P
DS26S10 N	MC26S10 P
DS26LS31 CJ	AM26LS31 DC
DS26LS31 CN	AM26LS31 PC
DS26LS32 CJ	AM26LS32 DC
DS26LS32 CN	AM26LS32 PC
DS3486 J	MC3486 L
DS3486 N	MC3486 P
DS3487 J	MC3487 L
DS3487 N	MC3487 P
DS3650 N	MC3450 P
DS3652 N	MC3452 P
DS75107 N	MC75107 P
DS75108 N	MC75108 P
DS3695 N	SN75176 N
DS3697 N	SN75177 N
DS3698 N	SN75178 N
DS8T26 AJ	MC8T26 AL
DS8T26 AN	MC8T26 AP
DS8T28 J	MC8T28 L
DS8T28 N	MC8T28 P

COMPETITION CROSS REFERENCE	
AMD	*Motorola Direct Replacement*
AM1488XC	MC1488L
AM1488PC	MC1488P
AM1489XC	MC1489L
AM1489PC	MC1489P
AM1489AXC	MC1489 AL
AM1489APC	MC1489AP
AM26S10PC	MC26S10P
AM26LS31DC	AM26LS31DC
AM26LS31PC	AM26LS31PC
AM26LS32DC	AM26LS32DC
AM26LS32PC	AM26LS32PC
AM3448ADC	MC3448AL
AM3448APC	MC3448AP
N8T26AB	MC8T26AP
N8T26AF	MC8T26AL
N8T28B	MC8T28P
N8T28F	MC8T28L

COMPETITION CROSS REFERENCE	
Fairchild	*Motorola Direct Replacement*
75107 APC	MC75107 P
75108 APC	MC75108 P
75110 APC	MC75S110 P
9636 ATC	MC3488AP1
9640 PC	MC26S10 P
μA1488 DC	MC1488 L
μA1488 PV	MC1488 P
μA1489 ADC	MC1489 AL
μA1489 APC	MC1489 AP
μA1489 DC	MC1489 L
μA1489 PC	MC1489 P
μA3448 ADC	MC3448 AL
μA3448 APC	MC3448 AP
μA3488 DC	MC3486 L
μA3486 PC	MC3486 P
μA3487 DC	MC3487 L
μA3484 PC	MC3487 P
μA96172 PC/DC	SN75172 N/J
μA96173 PC/DC	SN75173 N/J
μA96174 PC/DC	SN75174 N/J
μA96175 PC/DC	SN75175 N/J
μA96176 PC/DC	SN75176 N/J
μA96177 PC/DC	SN75177 N/J
μA96178 PC/DC	SN75178 N/J
μA8T26 ADC	MC8T26 AL
μA8T26 APC	MC8T26 AP
μA8T28DC	MC8T28 L
μA8T28 PC	MC8T28 P

COMPETITION CROSS REFERENCE	
Signetics	*Motorola Direct Replacement*
N8T26AF	MC8T26AL
N8T26AN	MC8T26AP
N8T28F	MC8T28L
N8T28N	MC8T28P
N8T95F	MC8T95L
N8T95N	MC8T95P
N8T96F	MC8T96L
N8T96N	MC8T96P
N8T97F	MC8T97L
N8T97N	MC8T97P
N8T98F	MC8T98L
N8T98N	MC8T98P